REMARKS

Claims 23-31 and 34-43 are pending. Claims 1-22, 32 and 33 are cancelled.

It is noted that the Examiner erroneously examined claims 1-21 replaced in a Preliminary amendment with claims 23-43. As the claims 23-43 differ from the amended claims 1-21 only in that they don't have reference numbers, the Applicant addresses the issues raised by the Examiner in the present response.

To avoid confusion, the new claim numbers corresponding to the claims addressed by the Examiner are indicates in brackets.

Claim 8 (new claim 30) has been objected to because the Examiner requested an article "a" before the words "connecting relation." The claim has been amended per the Examiner's request.

Claim 14 (new claim 36) has been objected to because the Examiner requested the words "state holding portion" in the next to the last line to be replaced with "state holding circuit." The claim has been amended per the Examiner's request.

Claims 13-15 and 20 (new claims 35-37 and 42) have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

The Examiner contends that the words "said reconfigurable unit" used in these dependent claims has insufficient antecedent basis because the respective independent claim 12 (new claim 34) recites "a plurality of reconfigurable units." In response, the rejected claims have been amended to change the word "said reconfigurable unit" to "a reconfigurable unit."

Claims 1-8 and 10-20 (new claims 23-30 and 32-42) have been rejected under 35 U.S.C. 102(b) as being anticipated by Abramovici. Dependent claims 9 and 21 (new claims 31 and 43) have been rejected under 35 U.S.C. 103 as being unpatentable over Abramovici in view of Mansingh.

Anticipation, under 35 U.S.C. § 102, requires that each element of a claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference. ***Kalman v. Kimberly-Clark Corp.,*** 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983); ***Richardson v. Suzuki Motor Co.,*** 868 F.2d 1226, 9 USPQ2d 1920 (Fed. Cir. 1989) *cert. denied,* 110 S.Ct. 154 (1989). The term "anticipation," in the sense of 35 U.S.C. 102, has acquired the accepted definition meaning "the disclosure in the prior art of a thing substantially identical with the claimed invention." ***In re Schaumann***, 572 F.2d 312, 197 USPQ 5 (CCPA 1978).

As demonstrated below, Abramovici does not disclose all elements of the independent claims 23 and 34.

In particular, claim 23 recites a processing device, comprising:

-a reconfigurable circuit allowing change in function;

-a first path portion transmitting an output of said reconfigurable circuit as an input to said reconfigurable circuit;

-a setting portion supplying setting data for configuring an intended circuit in said reconfigurable circuit;

-a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit, so that an output of a circuit configured on said reconfigurable circuit in accordance with one setting data is supplied to an input of a circuit configured in accordance with next setting data through said first path portion; and

-an internal state holding circuit receiving an output of said reconfigurable circuit, said internal state holding circuit being connected to said first path portion;

Said device further comprises:

-a memory portion storing in a prescribed area an output of a circuit configured on said reconfigurable circuit in accordance with said one setting data; and

-a second path portion transmitting the output of the circuit configured on said reconfigurable circuit stored in said prescribed area of said memory portion as an input to a circuit configured in accordance with the next setting data.

Considering the reference, Abramovici discloses a set of reconfigurable hardware 20 including a page manager (PAGMAN) 22 that controls four field programmable gate arrays (FPGAs) and communicates with a local memory 24 over a bus 23.

The Examiner considers the local memory 24 to correspond to the claimed memory portion, and takes the position that the bus 23 performs the claimed functions of the second path, i.e. transmits the output of the circuit configured on the reconfigurable circuit stored in the memory portion as an input to a circuit configured in accordance with the next setting data.

It is respectfully submitted that the reference does not support the Examiner's position. Abramovici discloses that the bus 23 provides communication between the RAM 24, the PAGMAN 22 and the FPGAs. However, the reference does not disclose that the bus 23 transmits the output of the circuit configured on the reconfigurable circuit stored in the memory as an input to a circuit configured in accordance with the next setting data.

It is noted that the processing device of claim 23 is characterized by comprising, as the path portion to transmit the output of the reconfigurable circuit as an input, a path portion (29) passing through a memory portion (27) corresponding to "second path portion," and a path portion (24) not passing through memory portion 27, corresponding to "first path portion".

Such a configuration enables high speed feedback processing using path portion (24) not passing through memory portion (27). In other words, the present invention provides advantage

of allowing a configuration of a predetermined high speed circuit based on high speed feedback processing.

Abramovici provides no disclosure or suggestion of a configuration including two path portions connecting the output and input of a reconfigurable circuit. i.e. "second path portion" passing through the memory portion, and "first path portion" not passing through the memory portion.

Hence, the subject matter of claim 23 is not anticipated by Abramovici.

Independent claim 34 recites a processing device, comprising:

-a reconfigurable circuit allowing change in function and connection relation;

-a setting portion storing setting data representing a divided unit forming a part of an intended circuit and supplying the setting data to said reconfigurable circuit; and

-a control portion controlling said setting portion such that a plurality of setting data are successively supplied to said reconfigurable circuit to configure said intended circuit; wherein

said reconfigurable circuit has at least one state holding circuit holding an internal state;

said reconfigurable circuit is divided, by an arrangement of said state holding circuit, into a plurality of stages of reconfigurable units; and

said control portion controls said setting portion such that when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow.

Claim 34 based on a configuration of the processing device corresponding, for example, to Fig. 25 of the present application, and is directed to configuration in which a plurality of

circuits differing in function are mapped simultaneously for execution of a plurality of operations in parallel.

Specifically, as illustrated, for example, in Fig. 30 of the present application, the setting portion sets circuits having a function different from each other as the first stage and the second stage of individual reconfigurable units simultaneously at a certain timing (first timing), and then the circuits as the second stage and third stage of the reconfigurable unit simultaneously at. the next timing (second timing).

Hence, a plurality of intended circuits can be configured in a reconfigurable circuit according to the sequence of the signal processing flow, thus providing the advantage of allowing high speed mapping of a plurality of intended circuits to realize a high speed logic operation. An addition advantage is in reducing the size and power consumption of the circuit by suppressing any waste in the reconfigurable unit and executing high speed processing.

By contrast, Abramovici discloses a configuration in which a plurality of FPGAs are provided. The page manager controls the loading and unloading for each page using respective FPGAs. However, Abramovici provides no disclosure or suggestion of the page manager dividing one reconfigurable circuit into a plurality of reconfigurable units, and setting a configuration of a circuit portion differing for each divided unit, as the claimed invention requires.

In particular, the reference does not disclose the claimed control portion that controls the setting portion such that when a plurality of intended circuits are to be configured, setting data for configuring divided units each forming a part of the circuits on respective ones of said plurality of stages of reconfigurable units are successively supplied along a process flow, as claim 34 recites.

Hence, Abramovici does not anticipate the subject matter of claim 34.

Dependent claims 24-31 and 35-43 are defined over the prior art at least for the reasons presented above in connection with the respective independent claims 23 and 34.

In view of the foregoing, and in summary, claims 23-31 and 34-43 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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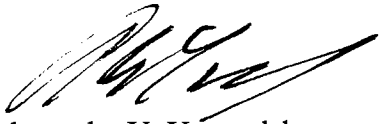

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